UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,956	12/20/2001	Benjamim Tang	35706.5700/65	5412

7590 02/07/2007

THEODORE E. GALENTHAY
PRIMARION, INC.
P.O. BOX 28308
SCOTTSDALE, AZ 85255-0155

EXAMINER	
TRUONG, LAN DAI T	
ART UNIT	PAPER NUMBER
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/029,956	TANG ET AL.	
	Examiner	Art Unit	
	Lan-Dai Thi Truong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to communications: application, filed 12/20/2001; amendment filed 08/18/2006. Claims 1-35 are pending; claims 1 and 10 are amended

Response to Arguments

2. According to applicant's arguments with respect to PLL/DLL loop data synchronous system comprising two loops interacting are persuasive. The previous rejection is withdrawn and all other arguments are moot in view of the new ground(s) of rejection.

Claims Objections

Claim 1 is objected to under 37 CFR 1.154 as being in confused form. Examiner does not clearly understand what part of the claim is preamble / and limitations such as what elements of the claim belong to "comprising" and what elements of the claim belong to "including." For examining purpose, Examiner assumes A PLL/DLL dual loop data comprising: a phase lock loop (PLL), a delay lock loop (DLL), a first-in first out (FIFO) register and a parallel-in serial-out (PISO) serializer. Then a phase lock loop (PLL) including: a phase frequency detector (PFD), a voltage controlled oscillator (VCO), a loop filter and a phase shifter

Claim 1 is objected according to "FIFO register", which is not supported by the specification.

Claim 17 is objected under 37 CFR 1.154 as being in confused form. Examiner does not clearly understand what part of the claim is preamble / and limitations

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or descry bed as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu (U.S. 6,901,126) in view of Filip (U.S. 6,081,572) in view of Drost et al. (U.S. 6,194,929) in view of Song (U.S. 6,639,956) and further in view of Schatz et al. (U.S. 6744787)

Regarding to claim 1:

Gu discloses the invention substantially as claimed, including a method, which can be implemented in a computer hardware or software code supports A PLL/DLL dual loop data senalizer comprising:

Communication between PLL and DLL, wherein phase lock loop (PLL) including, a phase frequency detector (PFD) receiving a local clock, a voltage controlled oscillator (VCO), a loop filter coupled to said PFD and to said VCO, said loop filter configured to suppress VCO phase noise: Gu discloses PLL comprises PFD, loop filter and VCO: (figure 3)

However, Go does not explicitly disclose phase shifter

In analogous art, Filip discloses correlations of executions between phase detectors with phase shifter and VCO: (column 5, lines 16-62)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Filip's ideas of including phase shifter with Gu's system in order to be able to generate delay signal from received original signal, see (Filip: column 5, lines 23-34)

However, Go- Filip does not explicitly disclose delayed lock loop (DLL) having a digital loop filter coupled to a phase detector

In analogous art, Drost discloses a delay-lock loop includes "a phase detector circuit" which is equivalent to "a phase detector," "a phase shift circuit" which is equivalent to " phase shifter:" (abstract, lines 1-7; column 3, lines 26-33; column 1, lines 45-67)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Drost's ideas of using DLL with Go- Filip's system in order to correct phases diffenences see (column 1, lines 46-59)

However, Go- Filip- Drost does not explicitly disclose a first-in first-out (FIFO) register receiving a parallel data input and outputting a signal to said phase detector;

In analogous art, Song discloses connection between phase detector and (FIFO) register: (column 6, lines 7-60)

However, Go- Filip- Drost - Song does not explicitly disclose a parallel-in serial- out (PISO) senalizer receiving an input from said FIFO and outputting serialized data

In analogous art, Schatz discloses PISO receives data from FIFO: (column 3, lines 1-56)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Schatz's ideas of interoperating executions of PISO and FIFO with Go- Filip- Drost – Song's system in order to generate the nominal clock rate, see (Schatz: column 3, lines 15-24)

Regarding to claim 2:

In addition to rejection in claim 1, Gu-Filip-Drost-Song-Schatz further discloses embedding between PLL and DLL: (Gu: figure 3)

Regarding to claims 3 and 6-7, 8-9:

This claim is rejected under rationale of claim 1

Regarding to claim 8-9:

This claim is rejected under rationale of claim 1, in light of Schatz and Gu

Claims 4-5 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost -Song-Schatz in view of Kirkpatrick (U.S. 6,476,681)

Regarding to claims 4-5:

Gu-Filip-Drost- Song-Schatz discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wideband filter and narrowband filter

In analogous art, Kirkpatrick discloses loop filter has different kinds of such as and filter and narrowband filter: (column 2, lines 32-44)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kirkpatrick's ideas of wideband filter and narrowband filter with Gu-Filip-Drost- Song-Schatz's system in order to be able to adjust bandwidth, see (Kirkpatrick: column 2, lines 32-44)

Claims 17-18 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost-Schatz-Song in view of Miller, Jr et al. (U.S. 6,316,976) further in view of Schmid et al. (6,735,291)

Regarding to claim 17:

Gu-Filip-Drost- Song-Schatz discloses the invention substantially as disclosed in claim 1, but does not explicitly teach DDLL

In analogous art, Miller discloses method of using DDLL: (abstract)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Miller's ideas of using DDLL with Gu-Filip-Drost- Song-Schatz's system in order to be able reset the delay of time, see (Schatz: column 3, lines 15-24)

However, Gu-Filip-Drost -Song-Schatz - Miller does not explicitly disclose SIPO

In analogous art, Schmid discloses each transmit circuit includes SIPO shift register, PISO shift register

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Schmid's ideas of interoperating executions of SIPO shift register, PISO shift register with Gu-Filip-Drost-Song-Schatz - Miller's system in order to be able transmit data stream from non-secure channels to secure channels, see (Schimid: column 9, lines 30-35)

Regarding to claims 18:

This claim is rejected under rationale of claim 17

Claims 19-22 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost –Song- Schatz -Miller- Schmid in view of Kirkpatrick (U.S. 6,476,681)

Regarding to claims 19 -22:

Gu-Filip-Drost- Song- Schatz -Miller- Schimid discloses the invention substantially as disclosed in claim 18, but does not explicitly teach wideband filter and narrowband filter

In analogous art, Kirkpatrick discloses loop filter has different kinds of such as and filter and narrowband filter: (column 2, lines 32-44)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kirkpatrick's ideas of wideband filter and narrowband filter with Gu-Filip-Drost- Song- Schatz -Miller- Schimid's system in order to be able to adjust bandwidth, see (Kirkpatrick: column 2, lines 32-44)

Claims 10-11, 16, 23-35 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost -Song -Schatz in view of Lennen (5,805,108) and further in view of Jaffe et al. (U.S. 2001/0034867) in view of Scala et al. (U.S. 4,551,689)

Regarding to claim 10:

Gu-Filip-Drost -Song-Schatz discloses the invention substantially as disclosed in claim 1, but does not explicitly teach detecting a local reference; suppress a phase noise of VCO

In analogous art, Lennen discloses local reference signal is detected: (column 18, lines 50-60)

However Gu-Filip-Drost -Song-Schatz -Lennen does not explicitly discloses filtering levels of FIFO

In analogous art, Jaffe discloses method for applying filtering method to FIFO: ([0072])

However, Gu-Filip-Drost -Song-Schatz -Lennen -Jaffe does not explicitly discloses phase shifting output from VCO in order to suppress phase noise

In analogous art, Scala discloses method using phase shifter to low phase noise signal: (abstract)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Lennen's ideas of detecting local reference with Jaffe's ideas of applying filtering method to FIFO with Scala's ideas of using phase shifter to low phase noise signal with Gu-Filip-Drost -Song-Schatz's system in order to provide frequency conversion for output signal: (Scala: abstract)

Regarding to claims 23 and 29:

Those claims are rejected under rationale of claims 1 and 17

Regarding to claims 11, 24-28, 30-35:

Those claims are rejected under rationale of claims 10, 23 and 29

Regarding to claim 16:

This claim is rejected under rationale of claim 10, in light of Schatz

Claims 12-13 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost -Song –Schatz-Lennen-Jaffe-Scala in view of Kirkpatrick (U.S. 6,476,681)

Regarding to claims 12-13:

Gu-Filip-Drost -Song –Schatz-Lennen-Jaffe-Scala discloses the invention substantially as disclosed in claim 10, but does not explicitly teach wideband filter and narrowband filter

In analogous art, Kirkpatrick discloses loop filter has different kinds of such as and filter and narrowband filter: (column 2, lines 32-44)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kirkpatrick's ideas of wideband filter and narrowband filter with

Gu-Filip-Drost -Song –Schatz-Lennen-Jaffe-Scala's system in order to be able to adjust bandwidth, see (Kirkpatrick: column 2, lines 32-44)

Claims 14-15 are rejected under 35 U.S.C 103(a) as being un-patentable over Gu-Filip-Drost -Song-Schatz-Lennen-Jaffe-Scala in view of Clark (U.S. 6,323,910)

Regarding to claims 14-15:

Gu-Filip-Drost -Song-Schatz-Lennen-Jaffe-Scala discloses the invention substantially as disclosed in claim 10, but does not explicitly translating into digital signal

In similar art, Clark discloses method for translating analog signals into digital signals

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Clark's ideas of translating analog signal into digital signals with Gu-Filip-Drost -Song-Schatz-Lennen-Jaffe-Scala's system in order to be able to process signal and adjust bandwidth, see (Kirkpatrick: column 2, lines 32-44)

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "PLL/DLL Dual loop data synchronization": 5,412,349; 6,738,922; 6,441,659; 6081572; 5805108

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/10/2006

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER